

結晶のみに限定して行けばならぬ問題にスミ
がある。これは、この形でも、この形でも行われ
その原因の一つは受光部以外に入射した光による
暗電流が、 $3/4$ に侵入することによる。

そこで、多量に結晶物を用いて素子を濃縮化す
ることによって、暗電流を大きく減減させ、さらに受光
素子に一定量を収めて $3/4$ 比を上げる方法が考
えられる。たとえば、付加容量として $5/10$ の $3/4$
などの濃縮を新たに収める方法がある。

(特許が解決しようとする問題点)

しかし前述の従来技術では受光素子や付加容量
を濃縮するのには新たに設備を収めてやらねばなら
ないために製造工程が増えてしまいコストが増加
するとともに、濃縮が均一に形成されにくいため
に雑音が増加することになる。

そこで本発明はこのような問題点を解決するも
ので、その目的とするところは、製造工程を増や
すことなく均一な付加容量を受光素子に並列に収
めた固体増倍装置を提供することにある。

る。受光素子及びエミッタ素子は半導体装置
ならばいかなるものであっても利用は可能であるが、こ
こでは受光素子として非晶質シリコンのフォトイ
ノード、エミッタ素子として多結晶シリ
コンを用いて代表させる。第2図は第1図の
下位回路である。第1図において(a)は前図、(b)
は本図であり、製造工程としては以下に示す様
になる。石英ガラスなどの絶縁基板 101 上にノ
ンドープの多結晶シリコン層 102 を形成、熱処理等
でポート絶縁層を形成後にポート電極となる第2
の多結晶シリコン層 103 を形成する。これら第2
ポート・エミッタともなる。その後カソード形成
等によりソースとドレイン電極を収める。次に電
解的処理 104 として $5/10$ などを形成した後、コン
タクトホールを形成し表面エミッタ 105 を $4/5$ などの
高濃度物質で形成し、その上に電解絶縁層を形成
して半導化のそのシリンドリカル構造を 106 として
形成する。以上は一般的な多結晶シリコンマ
ットの形成方法であり、これから本発明に關
して重要な第2工程である。電解絶縁層をシリ

コン絶縁層を形成するための工程！

本発明の固体増倍装置は、受光素子部分とエミ
ッタ部分として受光素子の下部電極の一部を酸化すること
で形成される濃縮層が上部電極との間で電圧を
蓄積すること、さらに均一な付加容量が形成さ
れ、並列に収めることができることを特徴とする。

または受光素子のフォトエミッタに濃縮層
のフロンガスを用いたシリコンエミッタ技術を用
いることで必然的にできる濃縮層を利用する。
また、受光素子部分に非晶質シリコンを用い、エ
ミッタ部分に多結晶シリコンを用いることでス
ミの少ない高感度かつ飽和電流の大きい固体増倍
素子となる。

(作用)

本発明の上記の構成によれば、受光素子の下部
電極に形成される濃縮層が下部電極と上部電極の
間で素子の付加容量となり、飽和電流を増やすこ
とに $3/4$ 比の低雑音固体増倍素子となる。

(実施例)

第1図は、本発明の増倍器における構成図であ

り、ホールを形成した後高濃度の下部電極として
 10^4 又は 10^5 などで高濃度層 107 を形成するが、こ
こではこの濃度は 10^6 の受光素子形成後にこの層を
（ホトレジストがついている場合もある）をノ
ズクトして 10^7 の高濃度層を酸化して付加容量
部 109 とするため、酸化が容易で酸化層が高濃度
で濃密でなくてはならない。酸化方法としては種
々の方法が考えられるが、 10^6 の受光素子形成
とフロンガスのプラズマでエミッタ化する場合は
必然的に酸化層 109 が形成され、なにも酸化工程を
増やす必要はない。この方法で酸化した後にさら
に酸化プラズマ処理したり、熱処理などで酸化し
てもよく、水素気酸化などもよい。本発明でこ
れらの酸化方法で 10^4 と 10^5 を下部電極 107 と
して形成の増倍例を第2図に示す。ここで、 10^4
の受光濃度はシリコンプラズマ 10^4 状態で形成した
多結晶シリコン（以下、 $a-b$ ）とすると、 10^5 は高
濃度層、上部電極 1 ならいかなるものであ
れ、ここでは 10^6 を用いている。

条 件	電子密度 $\times 10^7 / 100 \mu m^2$	絶縁性
(1) $CP_2 - O_2$ で $\alpha - Si$ を エッチング	0.2	良
(2) (1)に加えて O_2 プラズマ 処理	0.5	最 良
(3) (1)に加えて 熱酸化処理	0.5	良
(4) 電極に $Al - Si$ を用い (2)の条件	0.7	最 良
(5) 電極に $Al - Si$ を 用いて水素気で酸化	0.5	良

注) (1)～(3)の下層電極は Cr である。

第 1 表

第 1 表で電子密度は $\alpha - Si$ の密度と酸化膜の付着密度との和であるが、 $\alpha - Si$ の密度は $0.01 \times 10^7 / 100 \mu m^2$ 程度である。均一性に因しては、(3)の条件がもっとも良く全電子でのパッチは ± 1 以内であり、他は ± 2.5 以内である。いずれに

も(2)は断面図で、(3)は平面図である。

第 2 図は半導体の電極回路図である。

第 3 図は一般的な MOS 型固体撮像装置の回路図である。

- 101 基板
- 103 ゲート電極
- 105 垂直ライン
- 107 下層電極
- 108 受光層
- 109 酸化膜
- 110 上層電極

以 上

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てもこれらは Al_2O_3 層電極を別途形成するよりもむしろ著しく改善があり、パッチも少ない (50%の場合に ± 5 程度)。

第 2 図の電極回路であると、以上の工程により受光層上に Cr 層電極が正列に形成される。

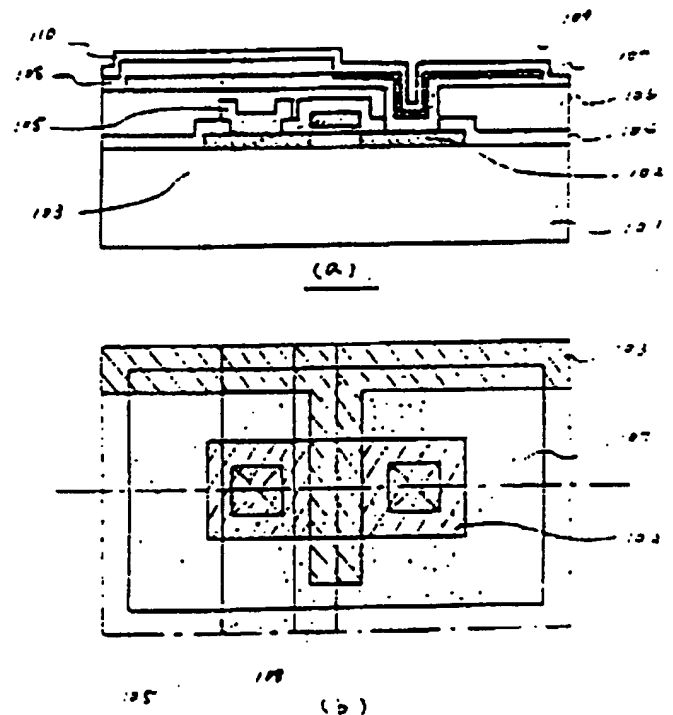
また上記例では下層電極として金属を用いたが、不純物ドーピングされた低抵抗結晶質シリコンを用いて、酸化を行ない SiO_2 を形成して電極層として用いることもできる。

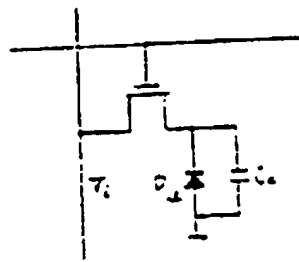
(電極の効果)

以上述べたように本発明によれば、高感度電子のパターンをマスクとすることで露光工程を省くことなく、著しく容易に均一性の高い電極層を形成できるために S/N 比が大きく、知覚能力の大きいすぐれた固体撮像装置を低コストで容易に構築することができる。

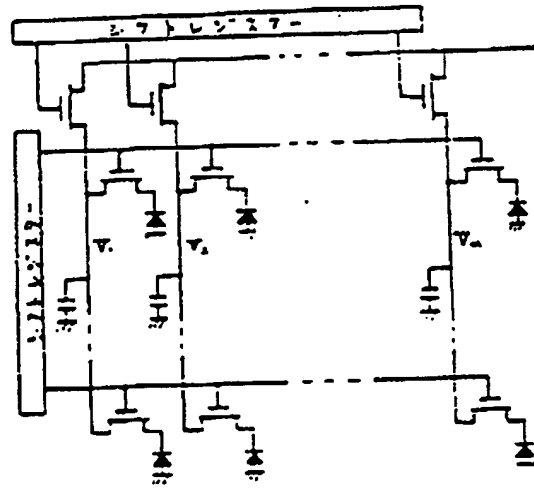
1. 図面の簡単な説明

第 1 図は本発明の固体撮像装置の構造例である。





第 2 図



第 3 図

documents are in the English language, and no concise explanation of those documents are required. Comments are, however, made on the Japanese documents 55-32026 and 61-141174 as follows:

The Japanese Patent Laid-Open No. 55-32026 teaches a liquid crystal device utilizing a semiconductor substrate. It teaches a necessity of planarizing a surface of the substrate in order to facilitate formation of an orientation control layer. Reference number 1 designates a semiconductor substrate, 4: transparent conductive film, 13: CVD SiO₂ film, 21: polyimide resin or low melting point glass layer.

The Japanese Patent Laid-Open No. 61-141174 is directed to a solid image sensor. It teaches an insulating substrate 101, non-doped polysilicon film 102, inter-layer insulating film 104 such as SiO₂, electrode 105, polyimide resin film 106.

The Rule 17(p) fee of \$240.00 is attached. Please consider these additional prior art documents.

JAPAN PATENT OFFICE (JP)

PATENT APPLICATION PUBLICATION

PATENT PUBLICATION OFFICIAL REPORT (A)

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1. Title of the Invention: Solid state image pickup device

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SPECIFICATION

1. Title of the Invention

Solid state image pickup device

5

2. Scope of Claim for Patent

1. A solid state image pickup device of a type of detecting an amount of stored/discharged charges by a light receptive element formed on an insulating substrate, characterized in that a capacitor is provided with an upper electrode in parallel with said light receptive element by oxidizing a portion of a lower electrode of the light
10 receptive element.

2. The solid state image pickup device according to claim 1 characterized in that an amorphous silicon is used as the light receptive element, chromium or aluminum is used as the lower electrode and an additional capacitance of an oxide film is formed simultaneously with photoetching the amorphous silicon film.

15

3. Detailed Description of the Invention

"Field of the Invention in Industry"

The present invention relates to a solid state image pickup device utilizing solid state image pickup elements.

"Prior art"

20

Conventionally, CCD type or MOS type is practicable as a solid state image pickup element. In compared with an image pickup tube, the solid state image pickup element is proof against vibration and clash. The solid state image pickup element is characterized in very little power consumption to be used for a long span. Further, MOS type has bigger numerical aperture and has no limit of the amount of transfer charge compared to CCD type, so that a lot of signal can be output. However, MOS type has a defect of occurring a great noise. Fig.

25

3 shows a drawing of typical MOS type circuit. Referring to the drawing, the cause of noise occurrence will be

described. The noise is caused by horizontal MOS FET switch which opens or closes a circuit. It is most serious problem, which causes in the case that a wiring capacitance on vertical lines V_1 to V_n is large and electrode-substrate capacitance of transistors formed on V_1 to V_n is large, so that noise charge which remains on the lines is read out. There is no comparison between the amount of noise and the capacitance of the receptive portion, so
5 that the S/N ratio is considerably decreased. In addition to the above mentioned problem of noise, there is one more problem of smear for both CCD type and MOS type. One of reasons is due to occurrence charge caused by light, which is incident upon the other portion in addition to the receptive portion, is signal lines.

Therefore, elements in thin film form is formed by utilizing an insulator as a substrate, so that wiring capacitance is considerably reduced. Further, S/N ratio is increased by forming additional capacitor on the
10 receptive element. For example, as the additional capacitor, a thin film such as SiO_2 or Y_2O_3 is deposited in addition.

"Problem To Be Solved by The Invention"

However, in the above mentioned prior art, an additional thin film has to be formed in order to connect a receptive element with an additional capacitor. Therefore, process steps will increase to cause cost up.
15 As a result, noise will be caused because a thin film will not be formed uniformly.

Therefore, the present invention will solve the problem. An object of the present invention is to provide a solid state image pickup device having an additional capacitor with high evenness in parallel with the receptive element without increasing the process steps.

"Means To Solve The Problem"

20 The solid state image pickup device in the present invention is characterized in that the additional capacitor with high evenness can be easily formed in parallel with the receptive element by a method wherein a part of lower electrode of receptive element is oxidized by utilizing receptive element portion as a mask to provide a capacitor between upper and lower electrodes.

In particular, the present invention is utilized an oxidation film formed by a method wherein receptive
25 element is performed photoetching by the technique of dry etching using Freon gas comprising oxygen. Moreover, the present invention utilizes an amorphous silicon for the portion of receptive element and a polycrystalline silicon

for the drive portion, respectively. Through these procedures, the solid state image pickup device having small amount of smear can be formed increasing sensitivity and saturated light quantity.

"Performance"

According to the above mentioned structure in the present invention, an oxidation film formed on lower electrode of a receptive element will be an additional capacitor between lower electrode and upper electrode. As a result, the solid state image pickup element having small noise will be formed increasing saturated light quantity and S/N ratio.

"Example"

Fig. 1 shows a configuration drawing in accordance with the present example of the present invention.

Any receptive element or switching element can be used for a semiconductor substrate. In the present invention, an amorphous silicon photodiode is used as a receptive element, and poly-silicon TFT is used as a switching element, respectively. Fig. 2 shows an equivalent circuit of Fig. 1. In Fig. 1, (a) shows a cross sectional view and (b) shows a plan view. Process steps will be described as follows. A non-doped polycrystalline silicon layer 102 is formed on an insulating substrate 101 such as quartz glass and after forming a gate insulating film by thermal oxidation, a second polycrystalline silicon 103 to be a gate electrode is formed to be also a gate line. Subsequently, ion is implanted to provide a source and drain electrode. Then, after forming SiO_2 or the like as an interlayer insulating film 104, a contact hole is formed and a vertical line 105 is formed with a conductive material such as Al, upon which a polyimide resin or the like 106 is formed for leveling as an interlayer insulating film. Usually, poly-silicon TFTs are formed by the above mentioned method. Significant process steps according to the present invention will be described as follows. After forming a contact hole on the interlayer insulating film, a conductive thin film 107 is formed by using such as Cr or Al as lower electrode of pixel. This conductive thin film 107 should be easily oxidized and the oxide film should be high resistivity and dense since it is oxidized after the formation of the receptive film 108 using the receptive film (a photo resist may be disposed thereon) as a mask in order to form an additional capacitor. As an oxidation method; it can be considered various kinds of method, however, in case that a receptive film 108 is etched by plasma using oxygen and Freon, an oxidation film 109 is formed as a necessary result, so that there is no need to add oxidation process. After oxidation by the method, oxide plasma

treatment may be further conducted, or oxidation with thermal nitric acid or steam oxidation may be conducted.

Table 1 shows a characteristic example of forming a lower electrode 107 by using oxidation of Cr and Al-Si and in accordance with the present example. Here, the receptive film thin 108 is an amorphous silicon (referred to a-Si, hereinafter) formed by GD plasma CVD, and 110 may be any transparent conductive electrode (upper electrode),

5 here, ITO.

Table 1

CONDITION	ELEMENT CAPACITY (pF/100 μ m ²)	INSULATION PROPERTY
(1) a-Si is etched by using CF ₄ +O ₂	0.2	good
(2) O ₂ plasma treatment in addition to (1)	0.5	best
(3) thermal nitrate treatment in addition to (1)	0.5	good
(4) using Al-Si as electrode with condition (2)	0.2	regular
(5) oxidation by steam using Al-Si as electrode	0.3	good

Note) An electrode used in conditions (1) to (3) is Cr.

10

In the table 1, an amount of the element capacity is calculated by adding capacitance of a-Si to additional capacitor of an oxidation film. The capacitance of a-Si is approximately 0.01pF/100 μ m². Regarding to the uniformity, the condition (3) is best of all. Under the condition (3), dispersion of all elements is within a range of \pm 1%, and under the other conditions, it is within a range of \pm 2.5%. In any way, it is easier than the case of forming SiO₂ or dielectric thin film in additional process and probability of dispersion is small. (in case of SiO₂, the dispersion is within a range of \pm 5%)

15

Referring to the equivalent circuit in Fig. 2, through the above mentioned process, the circuit is provided

with an additional capacitor Ca in parallel with the receptive element Dil.

Moreover, metal is used as a lower electrode in the above mentioned example. Instead of using the metal, by using low resistance amorphous silicon which is doped impurities, an oxidation may be performed to form SiO_2 in order to use the SiO_2 as an additional capacitor.

5 "The effect of the Invention"

As mentioned above, according to the present invention, since the additional capacitor having a high uniformity can be formed extremely easily and inexpensively without increasing the process steps by using the pattern of a thin film receptive element as a mask, it is possible to easily obtain excellent solid image pickup devices with low cost having a large S/N ratio and a large saturated light quantity.

10 4. Brief Explanation of The Drawings

Fig. 1 is example of a solid state image pickup device in the present invention wherein (a) is a cross sectional view and (b) is a plan view.

Fig. 2 is a equivalent circuit drawing of the example.

15 Fig. 3 is a usual circuit drawing of MOS type solid state image pickup device.

101---substrate

103---gate electrode

105---vertical line

20 107---lower electrode

108---receptive thin film

109---oxidation film

110---upper electrode

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